Accurate Harmonic Distortion Estimation in CMOS Circuits Using a Cross-Product G_m-Stage Modeling

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***Abstract*— This work presents a fast and flexible harmonic distortion estimation approach, applicable to linear CMOS circuits. It offers improved accuracy by using a G_m-stage model that includes the dependence of a stage's output current on cross-products of its input and output voltages. The application of the approach is demonstrated in a realistic circuit, and the accuracy of the obtained results is verified by comparison with Cadence® Spectre® simulation.**

I. Introduction

One of the most vital aspects of a circuit is harmonic distortion. It determines the quality characteristics of several devices, like audio and power amplifiers, low-noise amplifiers, filters, and many more.

Usually, the metric for distortion characterization is the total harmonic distortion (THD), that is the ratio of the power of all harmonics to the power of the fundamental. However, assuming that a circuit exhibits only smooth and weak non-linearities, the dominant distortion factors are HD_2 and HD_3

$$\mathrm{HD}_2 = \left|\frac{V_{h_2}}{V_f}\right|, \quad \mathrm{HD}_3 = \left|\frac{V_{h_3}}{V_f}\right| \tag{1}$$

where V_{h_k} is the amplitude of the k-th harmonic and V_f is that of the fundamental tone.

The estimation of harmonic distortion is usually performed via simulation, where methods like harmonic balance and shooting [1], [2] are exploited. Even though the obtained results are very accurate, little insight is gained, while the procedure is time-consuming. As such, dedicated methods for distortion prediction are favored for design optimization and parameterization.

A popular way to estimate the distortion behavior is by means of the Volterra series [3], but the difficulty of manipulating the method explodes with the number of circuit elements. Other methods include systematic time-domain state-space approaches [4]–[6], or algebraic manipulation of simplified amplifier models [7]–[11] in the frequency-domain. Nonetheless, most methods use CMOS stage models that cannot capture the distortion behavior accurately. [12].

In this paper, a time-domain approach to harmonic distortion estimation in CMOS circuits, with the use of a more involved G_m-stage model, is presented. The procedure has been implemented in MATLAB®, providing fast and accurate results.

The remainder of this paper is organized as follows. Section II presents the modeling of G_m-stages, and Section III deals with the harmonic distortion estimation procedure. The accuracy of the estimation is proven by comparison with Cadence® Spectre® simulation in Section IV, and conclusions are drawn in Section V.

II. Modeling CMOS Stages

Every CMOS stage that creates an output current due to an applied input voltage can be modeled as a G_m-stage, as shown in Figure 1. $G^m_{i,t,j}$ represents the G_m-stage that has positive input, u_i, negative input, u_t, and output current, i_{itj}, at node u_j. The G_m-stage's differential input voltage is denoted as $\widetilde{u}_{it} = u_i - u_t$. Notation subscript, itj, identifies a G_m-stage as a function of its input and output nodes.

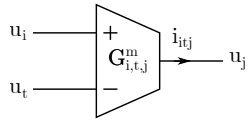

Fig. 1: G_m-stage representation.

The output current of a CMOS stage is generally a non-linear function of its input and output voltages. This non-linear nature causes distortion generation. It is reported that parasitic capacitors in MOS transistors do not have significant non-linearity contribution [13], [14]. This absence of frequency-related non-linearity makes possible the formation of an equivalent model based only on the DC-characteristics of a CMOS stage. Such a model results by the approximation of the stage's output current with a power-series expansion around its DC-operating point.

A. Frequently Used G_m-Stage Models

The simplest way to model the output current of a G_m-stage is to completely neglect its dependence on the stage's output

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voltage and take into account only power terms of the input voltage

$$i_{itj} = \sum_{k\geq 1} g_{itj,k}\widetilde{u}_{it}^{k}. \tag{2}$$

In (2), $g_{itj,k}$ is the model coefficient for each power, k, of $\widetilde{u}_{it}^{k}$. Although convenient to use, this model results in poor accuracy performance as it does not include any effect that depends on the output voltage.

A more appropriate model that is frequently used [7]–[11], results from the inclusion of both the input and output voltages of the stage in the power-series approximation of its output current

$$i_{itj} = \sum_{k\geq 1} \left(g_{itj,k}\widetilde{u}_{it}^{k} + \overline{g}_{itj,k}u_{j}^{k} \right) \tag{3}$$

where $g_{itj,k}$ and $\overline{g}_{itj,k}$ are the model coefficients for each power, k, of $\widetilde{u}_{it}^{k}$ and u_{j}^{k}, respectively. Assuming that the second and the third harmonic are the main contribution factors to the THD, it is normally set $k = 1, 2, 3$.

An advantage of the model of equation (3) is that the corresponding input- and output-related terms are independent of one another. However, the drain current of a MOS transistor depends on product terms of its gate-source and drain-source voltages [15]; the omission of such terms results in a less accurate expression for the transistor's drain current, which in turn can cause significant deviations in the predicted distortion generation of a G_m-stage.

B. Proposed Cross-Product G_m-Stage Model

Following the aforementioned reasoning, a G_m-stage model that also relates the stage's output current to cross-products of its input and output voltages is proposed. Analogous approximations exist at transistor-level [13], [14], [16], [17]; the MOS amplifying transistor is supposed to admit a two- or even three-dimensional Taylor series expansion, and the model coefficients of its approximation are calculated by means of the partial derivatives of the transistor's current relationship. A CMOS stage can be modeled in a similar way [12], [18]–[21].

In this work, the output current of each G_m-stage has a power-series approximation, in the time-domain [4]–[6], [22], of the form

$$i_{itj} = \sum_{\substack{k,\ell\geq 0 \\ k+\ell\geq 1}} g_{itj}^{k\ell}\widetilde{u}_{it}^{k}u_{j}^{\ell}. \tag{4}$$

In (4), the $k\ell$-superscript in the $g_{itj}^{k\ell}$-coefficients indicates the corresponding power k, of $\widetilde{u}_{it}^{k}$, and ℓ, of u_{j}^{ℓ}. Setting $k + \ell = 1, 2, 3$, to capture the major contributing terms to the fundamental, second and third harmonic, (4) reduces to

$$\begin{aligned} i_{itj} = {} & g_{itj}^{10}\widetilde{u}_{it} + g_{itj}^{20}\widetilde{u}_{it}^{2} + g_{itj}^{30}\widetilde{u}_{it}^{3} \\ & + g_{itj}^{01}u_{j} + g_{itj}^{02}u_{j}^{2} + g_{itj}^{03}u_{j}^{3} \\ & + g_{itj}^{11}\widetilde{u}_{it}u_{j} + g_{itj}^{21}\widetilde{u}_{it}^{2}u_{j} + g_{itj}^{12}\widetilde{u}_{it}u_{j}^{2}. \end{aligned} \tag{5}$$

C. G_m-Stage Model Coefficients

The $g_{itj}^{k\ell}$-coefficients are extracted by curve-fitting to take into account non-linearities that are amplitude-adjusted, instead of the locally-accurate Taylor expansion alternative that is suitable for small-amplitude signals. The coefficients can be derived through a three-step procedure. After the circuit is successfully formed as an interconnection of individual CMOS stages, an ac-analysis is performed to estimate the maximum expected signal amplitudes at the input and the output of each stage. These amplitude values mark the required voltage ranges for a 2-dimensional (2D) DC-sweep of the output current that follows, performed around each stage's input and output DC-operating points. Finally, the $g_{itj}^{k\ell}$-coefficients are extracted from the acquired data via linear regression, in the form of a linear least-squares problem [23].

III. Harmonic Distortion Estimation

Consider the general network of interconnected G_m-stages, resistors and capacitors, as shown in Figure 2, that is the equivalent representation of the circuit under consideration. Each node j, $j = 0, 1, \ldots, n$, may have a resistor, R_j, and a capacitor, C_j, connected to ground; possible coupling between nodes i and j can be provided by a capacitor, $\widetilde{C}_{ij}$. The signal current source, $\hat{i}_0$, is placed at node 0. For each node j, the current equation is

$$\hat{i}_j + \sum_{i,t} i_{itj} + \sum_{\ell} i_{\widetilde{C}_{\ell j}} = \frac{u_j}{R_j} + C_j\dot{u}_j, \quad \hat{i}_j = 0, j \neq 0. \tag{6}$$

In (6), $\sum_{i,t} i_{itj}$ is the sum of all G_m-stages' output currents that arrive at node j, and $\sum_{\ell} i_{\widetilde{C}_{\ell j}}$ is the sum of coupling currents arriving at or leaving node j, where

$$i_{\widetilde{C}_{ij}} = \widetilde{C}_{ij}\left(\dot{u}_i - \dot{u}_j\right) = -i_{\widetilde{C}_{ji}}. \tag{7}$$

Thus

$$\hat{i}_j + \sum_{i,t} i_{itj} + \sum_{\ell} \widetilde{C}_{\ell j}\dot{u}_{\ell} = \frac{u_j}{R_j} + \left(C_j + \sum_{\ell} \widetilde{C}_{\ell j} \right) \dot{u}_j. \tag{8}$$

Under the assumption of steady-state operation, the voltage of each node j can be written as a sum of fundamental and harmonic tones components

$$u_j = u_j^f + u_j^h \tag{9}$$

$$u_j^f = a_{j,1}\sin\omega t + b_{j,1}\cos\omega t \tag{9a}$$

$$u_j^h = a_{j,2}\sin 2\omega t + b_{j,2}\cos 2\omega t + a_{j,3}\sin 3\omega t + b_{j,3}\cos 3\omega t. \tag{9b}$$

The same holds for the signal current source, $\hat{i}_0$. For the harmonic distortion estimation, the fundamental tone coefficients, $a_{j,1}$ and $b_{j,1}$, are initially predicted for every node j of the circuit. Then, the estimation of the harmonic tones coefficients, $a_{j,2}$, $b_{j,2}$, $a_{j,3}$, and $b_{j,3}$, is made.

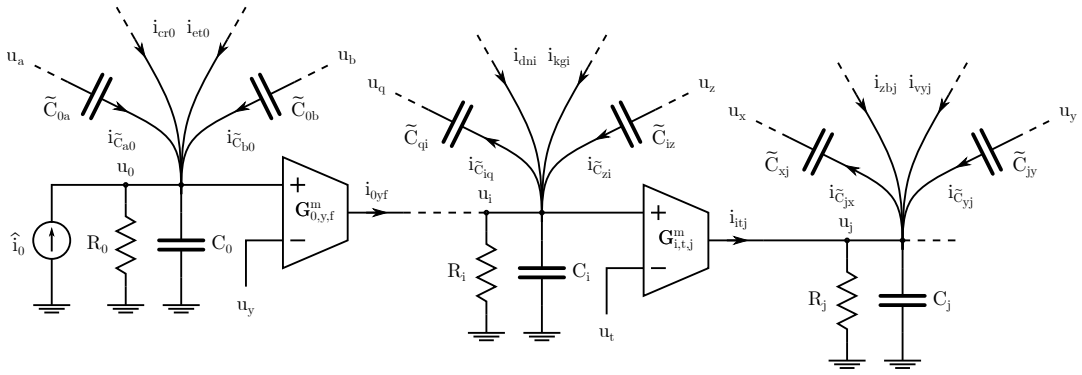

Fig. 2: General circuit structure, composed of G_m-stages.

A. Estimation of the Fundamental Tone

Since each G_m-stage is characterized by smooth and weak non-linearities, the contribution of the non-linear terms of (5) to the fundamental tone can be considered negligible. As such, only the linear terms of each i_{itj} are taken into account

$$i^f_{itj} = g^{10}_{itj}\widetilde{u}^f_{it} + g^{01}_{itj}u^f_j. \tag{10}$$

Including only the fundamental tone voltage component of (9a) in all involving voltages in (8), and setting up a system of equations for the complete circuit, the fundamental tone coefficients are directly derived by its solution.

B. Estimation of the Harmonic Tones

The harmonic tones components of (9b) are the result of the non-linear terms of (5). The calculation of all generated voltage terms in (5) results in a non-linear problem, that is computationally inefficient to solve. Inspecting (5) in association with (9) shows that the generated second and third harmonic tones coefficients will be a sum of

(a) products of only the fundamental tone coefficients,
(b) products of a single harmonic tone coefficient and one or more fundamental tone coefficients,
(c) products of harmonic tones coefficients of order higher that one.

Since the harmonic tones are anticipated to be much weaker than the fundamental tone, products (c) can be discarded without sacrificing accuracy. Thus, for the harmonic tones estimation, the expression of each i_{itj} is

$$i^h_{itj} = g^{10}_{itj}\widetilde{u}^h_{it} + g^{01}_{itj}u^h_j + p_{itj}\left(\widetilde{u}^f_{it}, u^f_j\right) + x_{itj}\left(\widetilde{u}_{it}, u_j\right) \tag{11}$$

where functions $p_{itj}\left(\widetilde{u}^f_{it}, u^f_j\right)$ and $x_{itj}\left(\widetilde{u}_{it}, u_j\right)$ include products (a) and (b), respectively. Note that all values of $\widetilde{u}^f_{it}$ and u^f_j are known from the solution of the fundamental tone coefficients in the previous step; that is, the problem of estimating the harmonic tones coefficients becomes linear.

Again, the system of equations for the complete circuit is formed (that is, equation (8) for $j = 0, 1, \ldots, n$), where only the harmonic tones voltage components are included in all involving voltages. The solution of the system yields the harmonic tones coefficients. Thus, HD_2 and HD_3 can be estimated for any node j

$$\mathrm{HD_2}^j = 10\log_{10}\left(\frac{a^2_{j,2} + b^2_{j,2}}{a^2_{j,1} + b^2_{j,1}}\right) \tag{12}$$

$$\mathrm{HD_3}^j = 10\log_{10}\left(\frac{a^2_{j,3} + b^2_{j,3}}{a^2_{j,1} + b^2_{j,1}}\right). \tag{13}$$

IV. Simulation Results

The proposed harmonic distortion estimation approach is implemented in MATLAB®, and is evaluated against Cadence® Spectre® parametric PSS-analysis in TSMC® $0.18\,\mu\mathrm{m}$ technology, for the two-stage open-loop amplifier of Figure 3. The amplifier has a DC-gain of $71.55\,\mathrm{dB}$ and a unity-gain frequency of $5.57\,\mathrm{MHz}$, under a load of $10\,\mathrm{k\Omega} \parallel 10\,\mathrm{pF}$.

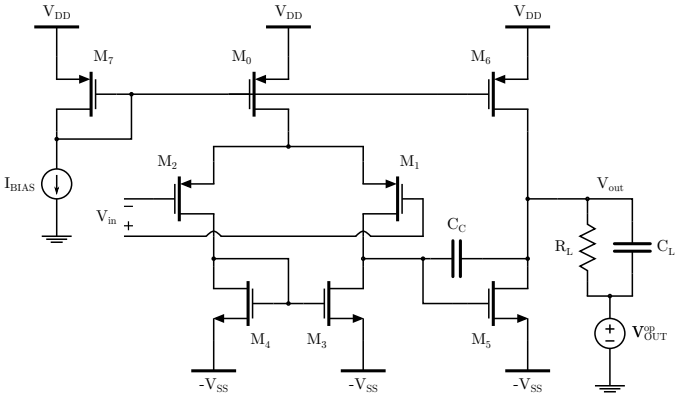

Fig. 3: Two-stage open-loop amplifier.

The G_m-stage representation of the amplifier is shown in Figure 4. The differential-pair of M_0-M_5 forms $G^m_{0,r,1}$, while the common-source (CS) stage of M_6-M_7 forms $G^m_{1,r,2}$ (r denotes the ac-ground). R_L is R_2, C_L is C_2, C_C is $\widetilde{C}_{12}$, and C_1 is the estimated parasitic capacitance at the differential-pair's output node. The input signal, V_{in}, is modeled by the current source $\hat{i}_0$ that acts on the normalized $R_0 = 1\,\Omega$.

For an input signal amplitude of $125\,\mu\mathrm{V}$ peak, Table I summarizes the extracted values for all $g^{k\ell}_{itj}$-coefficients. The

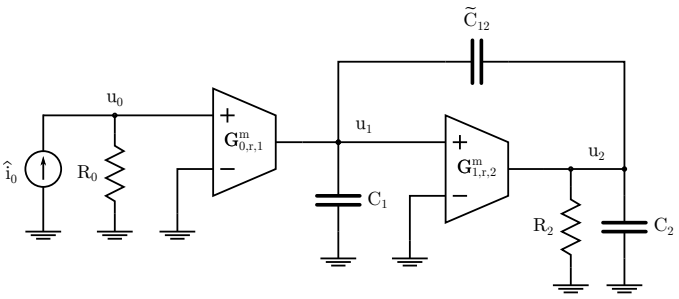

Fig. 4: G_m-stage equivalent representation of the two-stage open-loop amplifier.

predicted HD_2 and HD_3 behavior of each of the two stages is depicted in Figures 5, 6, 7 and 8, alongside with the results obtained by Cadence® Spectre®.

It can be seen that the estimation is in fine agreement with the simulation results; the error for HD_2 up to the unity-gain frequency of the amplifier is less than $0.67\,\mathrm{dB}$ and $2.55\,\mathrm{dB}$, for the differential-pair and the CS stage, respectively. The corresponding errors for HD_3 above the plateau of $-140\,\mathrm{dB}$ (that practically marks negligible harmonic distortion) are $1.59\,\mathrm{dB}$ and $1.71\,\mathrm{dB}$.

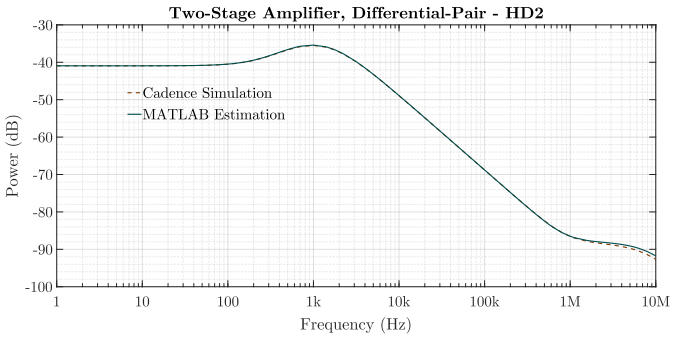

Fig. 5: HD_2 of the differential-pair.

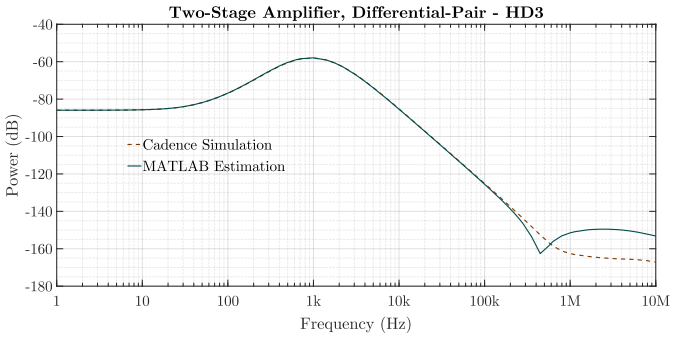

Fig. 6: HD_3 of the differential-pair.

V. Conclusion

In this paper, an approach to accurate estimation of harmonic distortion in CMOS circuits is presented. A more involved G_m-stage model is used, where the dependence of the stage's output current on cross-products of its input and output voltages is taken into account. The proposed approach is implemented in MATLAB® and applied to a two-stage amplifier case. The obtained results are in fine agreement with the ones from Cadence® Spectre® simulation, validating the accuracy of the estimation.

TABLE I: Extracted $g^{k\ell}_{itj}$-coefficients of the two stages.

$g^{k\ell}_{0r1}$	Value	$g^{k\ell}_{1r2}$	Value	Units
g^{10}_{0r1}	$-3.8133\cdot10^{-4}$	g^{10}_{1r2}	$-1.2433\cdot10^{-3}$	A/V
g^{20}_{0r1}	$-9.3399\cdot10^{-6}$	g^{20}_{1r2}	$-1.4786\cdot10^{-3}$	A/V^2
g^{30}_{0r1}	$-3.4743\cdot10^{-3}$	g^{30}_{1r2}	$+8.0996\cdot10^{-4}$	A/V^3
g^{01}_{0r1}	$-1.1933\cdot10^{-6}$	g^{01}_{1r2}	$-5.1056\cdot10^{-6}$	A/V
g^{02}_{0r1}	$+5.3020\cdot10^{-7}$	g^{02}_{1r2}	$-2.3688\cdot10^{-6}$	A/V^2
g^{03}_{0r1}	$-6.2335\cdot10^{-7}$	g^{03}_{1r2}	$-3.5850\cdot10^{-6}$	A/V^3
g^{11}_{0r1}	$-2.0239\cdot10^{-6}$	g^{11}_{1r2}	$-1.1713\cdot10^{-5}$	A/V^2
g^{21}_{0r1}	$+2.3208\cdot10^{-6}$	g^{21}_{1r2}	$+6.1709\cdot10^{-6}$	A/V^3
g^{12}_{0r1}	$+2.1916\cdot10^{-6}$	g^{12}_{1r2}	$-1.0589\cdot10^{-5}$	A/V^3

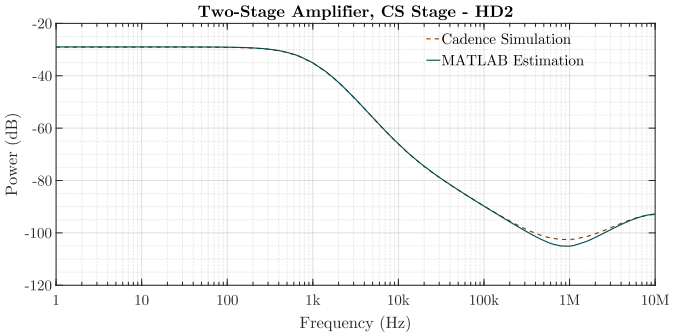

Fig. 7: HD_2 of the CS stage.

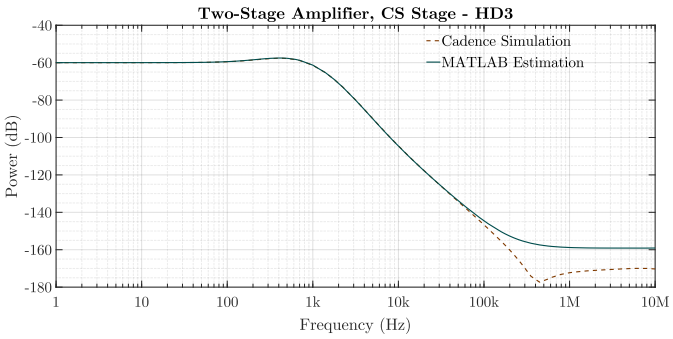

Fig. 8: HD_3 of the CS stage.

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REFERENCES

[1] Rowan J. Gilmore and Michael B. Steer, "Nonlinear circuit analysis using the method of harmonic balance—a review of the art. part i. introductory concepts," *International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering*, vol. 1, no. 1, pp. 22–37, 1991.

[2] Stephen A. Maas, *Nonlinear Microwave and RF Circuits*, 2nd ed. Artech House, 2003.

[3] Piet Wambacq and Willy Sansen, *Distortion Analysis of Analog Integrated Circuits*, 1st ed., ser. The Springer International Series in Engineering and Computer Science. Springer US, 1998, vol. 451.

[4] Z. Zhang, A. Celik, and P. Sotiriadis, "A fast state-space algorithm to estimate harmonic distortion in fully differential weakly nonlinear g_m-c filters," in *2006 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2006, pp. 4 pp.–2956.

[5] Zhaonian Zhang, A. Celik, and P. P. Sotiriadis, "State-space harmonic distortion modeling in weakly nonlinear, fully balanced g_m-c filters-a modular approach resulting in closed-form solutions," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 1, pp. 48–59, Jan 2006.

[6] P. P. Sotiriadis, A. Celik, D. Loizos, and Z. Zhang, "Fast state-space harmonic-distortion estimation in weakly nonlinear g_m-c filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 1, pp. 218–228, Jan 2007.

[7] G. Giustolisi, G. Palumbo, and S. Pennisi, "Harmonic distortion in single-stage amplifiers," in *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*, vol. 2, May 2002, pp. II–II.

[8] G. Palumbo and S. Pennisi, "High-frequency harmonic distortion in feedback amplifiers: analysis and applications," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 3, pp. 328–340, March 2003.

[9] S. O. Cannizzaro, G. Palumbo, and S. Pennisi, "Accurate estimation of high-frequency harmonic distortion in two-stage miller otas," *IEE Proceedings - Circuits, Devices and Systems*, vol. 152, no. 5, pp. 417–424, Oct 2005.

[10] ——, "Distortion analysis of three-stage amplifiers with reversed nested-miller compensation," in *Proceedings of the 2005 European Conference on Circuit Theory and Design, 2005.*, vol. 3, Sep. 2005, pp. III/93–III/96 vol. 3.

[11] ——, "Distortion analysis of miller-compensated three-stage amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 5, pp. 961–976, May 2006.

[12] G. Shi, "Symbolic distortion analysis of multistage amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 1, pp. 369–382, Jan. 2019.

[13] Sanghoon Kang, Byounggi Choi, and Bumman Kim, "Linearity analysis of cmos for rf application," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 3, pp. 972–977, March 2003.

[14] B. Toole, C. Plett, and M. Cloutier, "Rf circuit implications of moderate inversion enhanced linear region in mosfets," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 2, pp. 319–328, Feb 2004.

[15] Tony Chan Carusone, David Johns, and Kenneth Martin, *Analog Integrated Circuit Design*, 2nd ed. John Wiley & Sons, Inc., 2011.

[16] B. Hernes and W. Sansen, "Distortion in single-, two- and three-stage amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 5, pp. 846–856, May 2005.

[17] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-lna with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, June 2008.

[18] P. S. Crovetti, "Finite common-mode rejection in fully differential nonlinear circuits," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 8, pp. 507–511, Aug. 2011.

[19] P. S. Crovetti and F. Fiori, "Finite common-mode rejection in fully differential operational amplifiers," *Electronics Letters*, vol. 42, no. 11, pp. 615–617, May 2006.

[20] F. Fiori and P. S. Crovetti, "Nonlinear effects of radio-frequency interference in operational amplifiers," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 49, no. 3, pp. 367–372, Mar. 2002.

[21] Y. Miao and Y. Zhang, "Distortion modeling of feedback two-stage amplifier compensated with miller capacitor and nulling resistor," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, pp. 93–105, Jan. 2012.

[22] B. Perez-Verdu, J. Cruz, B. Linares-Barranco, A. Rodriguez-Vazquez, J. L. Huertas, and E. Sanchez-Sinencio, "Nonlinear time-domain macromodeling of ota circuits," *IEEE International Symposium on Circuits and Systems*, vol. 1989, pp. 1441–1444 vol.2, May 1989.

[23] H. W. Sorenson, *Parameter Estimation: Principles and Problems*, ser. Control and Systems Theory. M. Dekker, 1980, vol. 9.